data and address content from at least one sector of a compact flash memory array pair ~~data and address content~~ that is transferred back to the host device.

B1 end

22. (Original) The apparatus as recited in claim 9, the computer readable program code devices of the compact flash controller continues to perform each of the data transfer operative elements until the data transfer is complete.

23. (Previously presented) The computer program product as recited in claim 17, the computer readable program code devices of the compact flash controller stands by waiting for a predetermined time period for the next data transfer operation.

24. (Original) The computer program product as recited in claim 23, the computer readable program code devices of the compact flash controller suspends any operative activity and waits until a request to execute a new command sequence to be detected, if the a predetermined time period elapses.

* * * R*E*M*A*R*K*S * * *

Applicants herewith submit this Response B in a bona fide attempt to advance the prosecution of this case and to answer each and every ground of rejection as set forth by the Examiner. Applicants respectfully request reconsideration of the above referenced patent application in view of the remarks as set forth below.

Rejections under 35 U.S.C. §103(a)

The Examiner has rejected claims 1 through 24 under 35 U.S.C. § 103(a) as being unpatentable over United States Patent Application Publication No. US 2003/0009607 A1 published on January 9, 2003 by Joe Chen (Chen) in view of United States Patent Application Publication No. US 2001/0007119 A1 published on July 5,

2001 by Kunihiro Katayama et al. (Katayama et al.). In rejecting claims 1, 9 and 17 the Examiner states that it would have been obvious to integrate flash memory partitioning and data transferring method of Katayama et al. with the system of Chen in order to allow the system to sort data by type within the flash memory through the creation of partitions in addition to giving the system the capability of interleaving data throughout the memory arrays. This rejection is respectfully traversed.

Applicants have carefully studied the cited references by Chen and Katayama et al. Applicants' independent claims 1, 9 and 17 recite method, structure and computer program product for detecting a plurality of compact flash memory arrays, partitioning each of the flash memory arrays in accordance to the parameters of the configuration information table stored in a read-only memory of the compact flash controller and translating the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array pair.

It is to be noted, as quoted by the Examiner, that Chen does not teach a flash memory comprising of a number of flash memory arrays, the partitioning of flash memory arrays of the transfer of data to a memory array pair. Thus, it is submitted that applicants' independent claims 1, 9 and 17, and dependent claims 2 through 8, 10 through 16 and 18 through 24, further defining the method and structure of parent claims 1, 9, and 17, distinguish over Chen and are non-obvious in view thereof.

Applicants' have carefully studied the reference by Katayama et al. Katayama et al. appears to transfer data between a host and a flash memory, via a flash control

circuit 4, Figs. 1 and 2, by changing a 32 bit word into four 8 bit segments and transferring the four 8 bit segments via data latches 51, 52, 53, and 54, figs. 10 and 11 between a host and four memory arrays. Katayama et al., in their Summary of the Invention, page 2, paragraph [0017], state that their apparatus uses a parallel arrangement of memory element groups and the file memory comprises means for dividing data blocks into combined blocks and an arbitrary combination of memory element groups equal in number to the unit size data. It appears, Fig. 1, that their flash memory consists of flash memory arrays 5 and file control circuit 4 controlled by controller 27, Fig. 2. Contrary to the Examiner's statement, the controller 27 disclosed by Katayama et al., pages 4 and 5, paragraphs [0059] through [0069] does not appear as recited by applicants claims 1,9 and 17, to partition each of the flash memory arrays in accordance to the parameters of a configuration information table stored in a read-only memory of the compact flash controller or determine which interface specification is to be used to transfer data, address information and control signals to and from a host device. In contrast, applicants' claims 1, 9 and 17 recites method and structure steps of detecting a plurality of compact flash memory arrays and partitioning each of the flash memory arrays in accordance to the parameters of the configuration information table stored in a read-only memory of the compact flash controller. Furthermore, applicants' novel claims 1, 9 and 17 recite method and structure for translating the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array pair.

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Katayama et al. transfer 32 bit data in parallel groups of four 8 bit blocks to four memory chips Figs. 8, 10 and 11, not as claimed by applicants to a corresponding memory array pair.

The reference by Katayama et al., especially the Abstract; Fig. 2; pages 3 and 4, paragraphs [0053] through [0056] and pages 4 and 5, paragraphs [0057] through [0069] are silent in this regard. It is respectfully submitted that applicants' independent claims 1, 9 and 17, and dependent claims 2 through 8, 10 through16 and 18 through 24, furthering defining the method and structure of parent claims 1, 9, and 17, distinguish over the reference by Katayama et al and claims 1 through 24 are non-obvious in view thereof.

Even Chen in view of the reference by Katayama et al. does not make obvious applicants' claimed method and structure recited by independent claims 1, 9 and 17 for detecting a plurality of compact flash memory arrays, partitioning each of the flash memory arrays in accordance to the parameters of the configuration information table stored in a read-only memory of the compact flash controller and translating the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array pair. Neither Chen nor Katayama et al., nor the combination thereof, teach or make obvious applicants' claimed method and structure recited in independent claims 1, 9 and 19, and further defined by dependent claims 2 through 8, 10 through 16 and 18 through 24, for detecting a plurality of compact flash memory arrays, partitioning each of the flash

memory arrays in accordance to the parameters of a configuration information table stored in a read-only memory of the compact flash controller and translate the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array pair. Both Chen and Katayama et al. are to noted for their silence in this regard.

In view of the above set forth arguments, it is respectfully submitted that independent claims 1, 9 and 17 and dependent claims 2 through 8, 10 through 16 and 18 through 24, further defining the method and structure of independent claims 1, 9 and 17, are non-obvious in view of and particularly distinguish over the prior art of the references by Chen in view of Katayama et al. and claims 1 through 24 are clearly allowable under 35 U.S.C. 103(a) in accordance with the principles of Graham vs. John Deere Co.

In view of the Examiners comments in regards to the combination of dependent claims 2-3, 10-11, and 18 -19; 4, 12 and 20; 5, 13 and 21; 6, 14 and 22 and 7-8, 15 -16 and 23-24 it is to be observed that these claims are dependent on independent claims 1, 9 and 17 and further define the method and structure therein. In view of the above set forth arguments regarding independent claims 1, 9 and 17, it is respectfully submitted that dependent claims 2 through 8, 10 through 16 and 18 through 24, further defining the method and structure of independent claims 1, 9 and 17, are non-obvious in view of and particularly distinguish over the prior art of the references by Chen and Katayama et al. and one in view of the other and are clearly allowable in addition to

parent claims 1, 9 and 17 under 35 U.S.C. 103(a) in accordance with the principles of Graham vs. John Deere Co.

In consideration of the Examiner's response to applicant's arguments, applicants submit that neither the reference of Chen nor the reference of Katayama et al. teach detecting a plurality of compact flash memory arrays, partitioning each of the flash memory arrays in accordance to the parameters of a configuration information table stored in a read-only memory of the compact flash controller and translating the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array pair. Both Chen and Katayama et al., and the combination thereof, are silent in this regard. Contrary to the Examiner's statement that is possible for Katayama et al. to be divided into only two memory arrays it is noted that it is necessary for the invention by Katayama et al. to transpose a 32 bit word into four 8 bit segments and transfer them in parallel to four memory chips. This is the essence of his invention that is different from applicants' claimed invention.

CONCLUSION

In summary, applicants have again reviewed the specification, drawing and claims and believe they are in condition for allowance. The Examiner has again rejected claims 1 through 24. In view of the arguments herein set forth, applicants respectfully submit that claims 1 through 24 distinguish over the art cited by the Examiner and are allowable. Applicant having answered each and every ground of

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rejection as set forth by the Examiner submits that the case is in condition for allowance and the same is respectfully solicited. Favorable action in that regard and passage of this case to issue are earnestly solicited.

If any questions should arise with respect to the above remarks, or if it would in any way expedite the prosecution of this case, applicants' attorney would appreciate a telephone call by dialing Area Code (408)-965-4001.

Respectfully submitted,

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